UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,725	02/26/2004	Michael W. Morrow	P18374	6814

25694 7590 02/27/2006

INTEL CORPORATION
P.O. BOX 5326
SANTA CLARA, CA 95056-5326

EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 02/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,725	MORROW, MICHAEL W.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-20 are presented for examination. This office action is in response to the application filed on 2/26/2004.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 2/26/04 is being considered by the examiner.

The examiner requests, in response to this Office action, any reference(s) known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. That is, any prior art (including any products for sale) similar to the claimed invention that could reasonably be used in a 102 or 103 rejection. This request does not require applicant to perform a search. This **request** is not intended to interfere with or go beyond that **required** under 37 C.F.R. 1.56 or 1.105.

The request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request that are included in the application's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this request and any information

disclosures beyond the scope of this are subject to the fee and certification requirements of 37 CFR section 1.97.

In the event prior art documentation is submitted, a discussion of relevant passages, figs. etc. with respect to the claims is requested. The examiner is looking for specific references to 102/103 prior art that identify independent and dependent claim limitations. Since applicant is most knowledgeable of the present invention and submitted art, his/her discussion of the reference(s) with respect to the instant claims is essential. **A response to this inquiry is greatly appreciated.**

The examiner also requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s), in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title should be more specific to differentiate the invention from similar inventions in the patent literature. " instruction cache lines mixed with trace cache lines" and "cache lines are dynamically changing with time" aspects of the invention should be mentioned in the title so that the title is more descriptive.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Hironaka et al. (Hironaka) US Patent Pub. No. 2004/0088489.

As to claims 1 and 10, Hironaka discloses a storage device, comprising: a cache array having cache lines filled with contiguous instructions in an instruction cache (ICache) portion (Fig. 11 Ref. 30 and Fig. 14) that is adjacent to a trace cache (TCache) portion where cache lines are filled with elements of a trace (Fig. 11 Ref. 30).

As to claim 2, Hironaka further discloses an indexing logic where the ICache portion is looked-up when the TCache portion is not supplying instructions (Fig. 13, hit judgment circuit).

As to claim 3, Hironaka further discloses wherein neither the ICache portion nor the TCache portion is looked-up when the TCache portion is supplying instructions (Fig.

13, hit judgment circuit).

As to claim 4, Hironaka further discloses a line in the TCache portion is indexed when a branch instruction is executed (Fig. 11 and Fig. 13).

As to claim 5, Hironaka further discloses the TCache portion contains non-contiguous instructions from an instruction stream (Fig. 11, branch predictor read on this limitation since a branch address is not sequential, see Fig. 14).

As to claim 11, Hironaka further discloses dynamically changing a number of lines in the ICache portion and the TCache portion (Fig. 11, integrated reads on this limitation).

As to claim 12, Hironaka further discloses dynamically altering a size of the ICache portion and the TCache portion in the one array as time progresses (Fig. 11).

As to claim 13, Hironaka further discloses supplying a program-order stream of instructions from each cache line in the TCache portion (Figs. 11 and 14, instruction cache).

As to claim 14, Hironaka further discloses supplying instructions in program order from cache lines in the ICache portion until a branch is encountered (Figs. 11 and Fig.

14).

As to claim 15, Hironaka further discloses associating a next address with the first cache line in the TCache portion to allow a next line to be ready before a current line is completely fetched (block 7. parallel processing).

As to claim 6, Hironaka discloses a system, comprising: a processor (Fig. 1 Ref. 1); first and second antennas to receive modulated signals and supply a signal to the processor (examiner did not give any patentable weight because the recitation occurs in the preamble) and a cache having in one array both an instruction cache (ICache) portion (Fig. 11 Ref. 30 and Fig. 14) and a trace cache (TCache) portion (Fig. 11 Ref. 30), where a line in the TCache portion is indexed when the processor takes a branch (Fig. 11 ref. 31).

As to claim 7, Hironaka further discloses the TCache portion is further indexed when the processor takes a jump, a call or a return (Fig. 11 Ref. 31).

As to claim 8, Hironaka further discloses including an indexing logic where the ICache portion is looked-up when the TCache portion is not supplying instructions (Fig. 13, hit judgment circuit).

As to claim 9, Hironaka further discloses the indexing logic is not used for either the ICache portion or TCache portion when the TCache portion is supplying instructions (Fig. 13, hit judgment circuit).

As to claim 16, Hironaka discloses a method comprising: using one control circuit to fill an array with instruction cache (ICache) cache lines mixed with trace cache (TCache) cache lines (Fig. 11 Ref. 30) where an allocated proportion of ICache cache lines to TCache cache lines is dynamically changing with time (Fig. 14).

As to claim 17, Hironaka further discloses using an address of a next instruction when an end of a cache line is reached to determine use of the ICache cache lines or the TCache cache lines (Fig. 13).

As to claim 18, Hironaka further discloses searching both the ICache cache lines and the TCache cache lines when an address is a result of a branch target (Fig. 13 judgment circuit and Fig. 14).

As to claim 19, Hironaka further discloses using the TCache cache lines when an address is found in the TCache cache lines (Fig. 13 judgment circuit).

As to claim 20, Hironaka further discloses using the ICache cache lines when the address is found in the ICache cache lines and not in the TCache cache lines (Fig. 13 judgment circuit).

5. Claims 1, 10 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (Wang) US Patent Pub. No. 2002/0144101.

As to claims 1, 10 and 16, Hironaka discloses a storage device, comprising: a cache array having cache lines filled with contiguous instructions in an instruction cache (ICache) portion that is adjacent to a trace cache (TCache) portion where cache lines are filled with elements of a trace (block 14 bottom), where an allocated proportion of ICache cache lines to TCache cache lines is dynamically changing with time (block 14 bottom).

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
571-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

HK
Primary Patent Examiner
February 19, 2006